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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/523,257	01/27/2005	Elstan Anthony Fernandez	2002 P 05725 US	8306

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EXAMINER	
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ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/523,257	FERNANDEZ, ELSTAN ANTHONY	
	Examiner	Art Unit	
	Thanh Y. Tran	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,9-12,14-17 and 19-25* is/are pending in the application.

4a) Of the above claim(s) *10-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 9, 14-17, 19-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/9/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Applicant's election with traverse of group I, claims 1-6, 9, 14-17 and 19-25 which was filed on 7/5/07 is acknowledged. The traversal is on the ground(s) that it is not burdensome to examine all pending claims. This traversal is not persuasive because the inventions are classified in different classes and there are divergent subject matters and the search for a semiconductor package in group I does not require the same search as the method in group II.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4, 9, 14, and 20-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Vaiyapuri (U.S. 2002/0027271).

As to claim 1, Vaiyapuri discloses in figure 2 a semiconductor package including a substrate (190), an integrated circuit (120) mounted on the substrate (190), a heat conductive plate (comprising 116, 108, 192) having a first portion (116) including a central region interposed between the integrated circuit (120) and the substrate (190), the central region (116) heat-conductively connected to the integrated circuit (120) and the heat conducting plate having at least one second portion (192) extending laterally out from the central region (116) between the integrated circuit (120) and the substrate (190); and a second integrated circuit (130) disposed

between the plate (comprising 116, 108, 192) and the substrate (190), the plate being in heat-conductive contact with the second integrated circuit (130), whereby heat generated by the second integrated circuit (130) is conducted away from the second integrated circuit (130) by the plate.

As to claim 2, Vaiyapuri discloses in figure 2 a semiconductor package in which the integrated circuit (120/130) is encased in resin (176), the plate extending out of the resin (176), whereby heat generated in the integrated circuit (120/130) is conducted out of the resin (176).

As to claim 3, Vaiyapuri discloses in figure 2 a semiconductor package, comprising: the second portion (192) includes arms extending laterally from the central region (116) with openings between them, the integrated circuit (120/130) being connected to the substrate (190) by wire bonding (160) in the openings.

As to claim 4, Vaiyapuri discloses in figure 2 a semiconductor package, wherein the integrated circuit (120/130) has a substantially square or rectangular profile and where at least one of the arms (142, 152) extends in a direction which is diagonal relative to the square or rectangular profile of the integrated circuit (120/130).

As to claim 9, Vaiyapuri discloses in figure 2 a semiconductor package in which the second integrated circuit (130) is a flipchip.

As to claim 14, Vaiyapuri discloses in figure 2 a packaged semiconductor device comprising: a substrate (190) including a plurality of contact regions (contact regions are the contact regions between surfaces of the substrate 190 and element 192) on an upper surface; a heat conductive plate (comprising 116, 108, 192) mounted over the substrate (190), the heat conductive plate comprising a central portion (116) and a plurality of arms (152, 142) extending

outwardly from the central portion (116), one or more of the arms (152, 142) extending laterally outwardly from a side surface of the central portion (116) of the plate; an integrated circuit (120) having a bottom surface mounted over the central portion (116) of the heat conductive plate; and a plurality of electrical connections (160) between an upper surface of the integrated circuit (120) and the contact regions of the substrate (190), the electrical connections (160) extending between adjacent ones of the arms (152, 142) of the heat conductive plate.

As to claim 20, Vaiyapuri discloses in figure 2 a packaged semiconductor device, wherein the central portion (116) of the heat conductive plate is affixed to the integrated circuit (120) by heat-conductive glue ("adhesive") and wherein the central portion (116) of the heat conductive plate is affixed to the substrate (190) by heat-conductive glue (see paragraph [0025]).

As to claim 21, Vaiyapuri discloses in figure 2 a semiconductor package including: a substrate (190); an integrated circuit (120) mounted on the substrate (190); a heat conductive plate (comprising 116, 108, 192) having a first portion (116) interposed between the integrated circuit (120) and the substrate (190), the heat conductive plate being heat-conductively connected to, and electrically isolated from, the integrated circuit (120) and having at least one second portion (192) extending laterally out from between the integrated circuit (120) and the substrate (190); and a second integrated circuit (130) disposed between the plate and the substrate (190), the plate being in heat-conductive contact with the second integrated circuit (130), whereby heat generated by the second integrated circuit (130) is conducted away from the second integrated circuit (130) by the plate; wherein the plate includes a central region (116) disposed between the substrate (190) and the integrated circuit (120/130) and arms (142, 152)

extending laterally from the central region (116) with openings between them, the integrated circuit (120/130) being connected to the substrate (190) by wire bonding (160) in the openings.

As to claim 22, Vaiyapuri discloses in figure 2 a semiconductor package, wherein the integrated circuit (120/130) has a substantially square or rectangular profile and where at least one of the arms (142, 152) extends in a direction which is diagonal relative to the square or rectangular profile of the integrated circuit (120/130).

As to claims 23 and 25, Vaiyapuri discloses in figure 2 a semiconductor package, wherein the plate further comprises an attachment to attach to a heat dissipation device ("common die attach site", se paragraph [0041]).

As to claim 24, Vaiyapuri discloses in figure 2 a semiconductor package, comprising: attacking the plate to a heat dissipation device ("common die attach site", se paragraph [0041]).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vaiyapuri Vaiyapuri (U.S. 2002/0027271) in view of Ohsawa et al (U.S. 2002/0031862).

As to claim 6, Vaiyapuri does not disclose the plate includes at least one portion of increased thickness laterally outward from the integrated circuit.

Ohsawa et al discloses in figures 2A-2D a semiconductor package comprising a plate (comprising elements 2 and 3) includes at least one portion (3) of increased thickness laterally outward from the integrated circuit ("LSI chip" 7). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor package of Vaiyapuri by having a plate that includes at least one portion of increased thickness laterally outward from the integrated circuit as taught by Ohsawa et al for supporting the semiconductor package when the semiconductor package is mounted a motherboard.

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vaiyapuri (U.S. 2002/0027271) in view of Joshi (U.S. 4,069,498).

As to claim 5, Vaiyapuri does not disclose the plate is grounded and electrically connected to at least one ground input of the integrated circuit.

Joshi discloses in column 1, lines 36-39 a heat plate is grounded ("ground potential") and electrically connected to at least one ground input of the integrated circuit ("chip"). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor package of Vaiyapuri by having a heat plate is grounded and electrically connected to at least one ground input of the integrated circuit as taught by Joshi for providing a good heat mechanism or good electrical conductors, and enhancing the heat transfer from the chip (col. 1, lines 45-68 in Joshi)

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vaiyapuri (U.S. 2002/0027271) in view of Papageorge et al (U.S. 5,438,224).

As to claim 19, Vaiyapuri does not disclose a plurality of balls disposed on a lower surface of the substrate, each of the balls electrically coupled to a respective one of the contact regions.

Papageorge et al discloses in figure 1 a packaged semiconductor device comprising: a plurality of balls ("bumps" 159 disposed on a lower surface of the substrate (150), each of the balls (159) electrically coupled to a respective one of the contact regions (152). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Vaiyapuri by having a plurality of balls disposed on a lower surface of the substrate, each of the balls electrically coupled to a respective one of the contact regions as taught by Papageorge et al for coupling the IC assembly or semiconductor package to circuitry of the external circuit board (see col. 5, lines 40-53 in Papageorge et al).

7. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vaiyapuri (U.S. 2002/0027271) in view of Araki et al (U.S. 6,828,661).

A to claims 15-17, Vaiyapuri does not disclose the packaged semiconductor device, wherein the heat conductive plate further comprises a rim portion that surrounds the central portion and is thermally connected to the central portion by the plurality of arms, the heat conductive plate includes four diagonal arms, each diagonal arm extending outwardly from a corner of the central portion to the rim portion; and the heat conductive plate further includes

four lateral arms, each lateral arm extending outwardly from a side surface of the central portion of the plate to the rim portion.

Araki et al discloses in figure 2a a packaged semiconductor device, wherein the heat conductive plate (13) comprises a rim portion (13a) that surrounds the central portion (23b) and is thermally connected to the central portion (23b) by the plurality of arms (23c), the heat conductive plate (13) includes four diagonal arms (23c), each diagonal arm (23c) extending outwardly from a corner of the central portion (23b) to the rim portion (13a); and the heat conductive plate (13) further includes four lateral arms (23c), each lateral arm (23c) extending outwardly from a side surface of the central portion (23b) of the plate to the rim portion (13a). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the device of Vaiyapuri by including a rim portion that surrounds the central portion as taught by Araki et al for providing a sufficient mechanical strength or reliability of the resin-sealed semiconductor device (see col. 7, lines 32-59 in Araki et al).

Response to Arguments

8. Applicant's arguments with respect to claims 1-6, 9, 14-17, and 19-25 have been considered but are moot in view of the new ground(s) of rejection.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TYT

Zandra V. Smith
Supervisory Patent Examiner
17 Sept 2007